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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,964	02/04/2004	David Michael Anderson	200208842-1	3839

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,964	ANDERSON, DAVID MICHAEL	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,9,10 and 17-22* is/are rejected.

7)☒ Claim(s) *3-8, 11-16 and 23-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/04/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/771,964 filed on 02/04/2004. Claims 1-28 remain pending in the application.

Claim Objections

2. Claims 3, 11 and 23 are objected to because following informalities:

Applicant must clarify what is "said compatibility map (line 13 in claim 3)". Is this "a compatibility map derived from said port compatibility map" (lines 11-12 in claim 3) or "said port compatibility map" (lines 3-4 in claim 3)?

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 9-10, 17-20 and 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Schmitz (US Patent 5,128,871).

As to claims 1, 9, 17 and 21 Schmitz discloses:

(1) A method for providing interface compatibility between two hierarchical collections *("a different design library or ... another portion of the same library"- Application, paragraph 15)* of integrated circuit (IC) design objects, comprising (col.53, ll.45-55):

establishing an associative correspondence between a design object from a first hierarchical (assignment dependencies/fanout) collection and a design object from a second hierarchical collection (The product term resources in a programmable logic block may be thought of as the abilities of the males in the marriage problem. The logic equations (females) are "compatible" to the degree the macrocells have adequate product term resources present – col.54, ll.14-18) (col.54, ll.5-26; col.59, ll.11-29);

generating a port compatibility map based on determination that a particular associative correspondence includes a pair of design objects, one from each hierarchical collection, that are port-compatible (an initial mapping of the logic equations to the programmable logic block resources is created from the reduced matrix (FIG. 42D)- col.55, ll.10-11) (col.54, ll.54-68; col.55, ll.1-20); and

reducing said port compatibility map to determine a set of design object pairs that allow replaceability between said first and second hierarchical collections (briefly stated the assignment process systematically determines an optimal association between the two populations. In this case, an optimal assignment is a minimum sum of the compatibility measure across all pairs consisting of one member from each population- col.53, ll.59-64; the next step in the Hungarian assignment process is to find the minimum uncovered number M and use that number in a second reduction of the matrix ... In the second reduction, number M is first subtracted from all uncovered rows, i.e., rows B, C and E and then the number M is added to all covered columns i.e., columns W and Y- col.55, ll.58-65) (col.53, ll.56-66; col.55, ll.38-68; col.56, ll.1-3);

(9) system for providing interface compatibility between two hierarchical collections *("a different design library or ... another portion of the same library"- Application, paragraph 15)* of integrated circuit (IC) design objects, comprising (col.15, ll.34-51; col.53, ll.45-55):

means for establishing an associative correspondence between a design object from a first hierarchical collection and a design object from a second hierarchical collection (col.15, ll.26-33; col.54, ll.5-26; col.56, ll.23-62; col.59, ll.11-29);

means for generating a port compatibility map based on determination that a particular associative correspondence includes a pair of design objects, one from each hierarchical collection, that are port-compatible (col.54, ll.54-68; col.55, ll.1-20; col.56, ll.23-62); and

means for reducing said port compatibility map to determine a set of design object pairs that allow replaceability between said first and second hierarchical collections (col.53, ll.56-66; col.55, ll.38-68; col.56, ll.1-3; col.56, ll.23-62);

(17) computer platform operable support an integrated circuit (IC) chip design database environment, comprising:

a first and a second collection of design objects disposed in said IC chip design database environment (col.15, ll.34-51; col.53, ll.45-55; col.56, ll.16-22);

a port compatibility engine operating to generate a port-compatible group of design objects relative said first and second collections of design objects (col.4, ll.1-15; col.54, ll.5-26);

a compatibility engine for obtaining a compatible group of design objects based on said port-compatible group (col.4, ll.1-15; col.54, ll.54-68; col.55, ll.1-20); and

a reduction engine for iteratively reducing said compatibility group to a set of design objects that are replaceable between said first and second collections of design objects (col.4, ll.1-15; col.53, ll.56-66; col.55, ll.38-68; col.56, ll.1-3);

(21) A computer-accessible medium operable with a computer platform to support an integrated chip (IC) chip design database environment, the medium having stored thereon instructions for providing interface compatibility between two hierarchical collections of IC design objects, comprising (col.15, ll.34-51; col.53, ll.45-55):

program code for establishing an associative correspondence between a design object from a first hierarchical collection and a design object from a second hierarchical collection (col.15, ll.34-51; col.54, ll.5-26; col.59, ll.11-29);

program code for generating a port compatibility map based on determination that a particular associative correspondence includes a pair of design objects, one from each hierarchical collection, that are port-compatible (col.15, ll.34-51; col.54, ll.54-68; col.55, ll.1-20); and

program code for reducing said port compatibility map to determine a set of design object pairs that allow replaceability between said first and second hierarchical collections (col.15, ll.34-51; col.53, ll.56-66; col.55, ll.38-68; col.56, ll.1-3).

As to claims 2, 10, 18-20 and 22 Schmitz recites:

(2), (10), (22 The method/system/program for providing interface compatibility, wherein said operation of reducing said port compatibility map is performed iteratively (col.56, ll.4-16);

(18), (19) The computer platform, wherein said first and said second collection of design objects is hierarchically arranged (col.54, ll.5-26; col.59, ll.11-29);

(20) The computer platform, wherein each of said first and second collections of design objects comprises a standard cell library portion (col.5, ll.42-45).

Allowable Subject Matter

4. Claims 3-8, 11-16 and 23-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

A method/system/database/program for providing interface compatibility between two hierarchical collections as recited in claims 1 and 2, wherein said operation of reducing said port compatibility map further comprises: pruning design object entities of said port compatibility map based on determination that a specific design object at a particular hierarchical level is exchangeable between said first and second hierarchical collections regardless of whether any design objects respectively under said specific design objects are port- incompatible, thereby generating a compatibility map derived

from said port compatibility map; for each design object of said compatibility map whose Boolean value is false, determining if a user design object thereof can be falsified, wherein said user design object is a parent design object in said compatibility map whose Boolean value is true; if so, rendering said user design object's Boolean value to be false; and falsifying remaining design objects of said compatibility map until all parent design objects therein are exhausted, thereby arriving at a set of design objects whose Boolean values indicate whether they can be replaced between said first and second hierarchical collections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N L

THUAN DO
Primary examiner.
03/16/2006.